Amendments to the Claims

This listing of claim will replace all prior versions and listings of claim in the application.

1. (original) A memory module comprising:

a connector interface which includes a first contact and a second contact;

a first integrated circuit having memory including a first storage cell and a second storage cell; and

a buffer device coupled to the first integrated circuit and the connector interface, wherein the buffer device is operable in a first mode and a second mode, wherein:

during the first mode of operation, the first storage cell and the second storage cell are accessible from the first contact; and

during the second mode of operation, the first storage cell is accessible from the first contact and the second storage cell is accessible from the second contact.

2. (original) The memory module of claim 1, wherein the buffer device includes a configurable width interface to communicate with a controller device via the connector interface, wherein the configurable width interface is configured to include a first operable number of interface circuits in the first mode and a second operable number of interface circuits in the second mode.

3. (original) The memory module of claim 2, wherein upon initialization, the buffer device detects a width of an interface of the controller device, wherein the buffer device configures the configurable width interface based on the width of the interface of the controller device.

4. (original) The memory module of claim 2, wherein the memory module includes a programmable storage device, wherein a number of possible configurations of the configurable width interface are specified by information stored in the programmable storage device.

5. (original) The memory module of claim 4, wherein the programmable storage device is a serial presence detect device.

6. (original) The memory module of claim 2, wherein the buffer device includes a control terminal to receive information from the controller device that represents the width of the interface of the controller device, wherein the configurable width is programmed based on the information.

7. (original) The memory module of claim 1, wherein the buffer device includes a programmable register, wherein the first mode and the second mode are specified by respective values stored in the programmable register.

8. (original) The memory module of claim 1, wherein the buffer device includes a control terminal, wherein the first mode and the second mode are specified by asserting respective control signals on the control terminal.

9. (original) The memory module of claim 1, wherein the first mode of operation is a narrow width mode and the second mode of operation is a native width mode.

10. (original) The memory module of claim 1, wherein the first integrated circuit device includes:

a first transceiver circuit, to transfer data with the buffer device via a first external signal line disposed on the module;

a second transceiver circuit, to transfer data with the buffer device via a second external signal line disposed on the module;

a first internal data path coupled to the first transceiver circuit and the first storage cell;

a second internal data path coupled to the second transceiver circuit and the second storage cell; and

an addressable memory array including the first storage cell and the second storage cell, wherein the first storage cell is accessible via the first internal data path and the first transceiver and the second storage cell is accessible via the second internal data path and the second transceiver.

11. (original) The memory module of claim 10, wherein the first storage cell is a dynamic memory cell and the first transceiver circuit includes a transmitter to output data synchronously with respect to rising and falling edges of a clock signal.

12. (currently amended) The memory module of claim 1, wherein the buffer device includes a configurable serialization circuit coupled to the connector interface, and a first port and second port coupled to the integrated circuit, wherein the first port is coupled to access the first ~~memory~~ storage cell and the second port is coupled to access the second ~~memory~~ storage cell, wherein:

in the first mode, the configurable serialization circuit is configured to steer a data stream from the first contact to the both the first port and the second port; and

in the second mode, the configurable serialization circuit is configured to steer a first data stream from the first contact to the first port and a steer second data stream from the second contact to the second port.

13. (currently amended) The memory module of claim 1, wherein the first and second contacts are included in a plurality of contacts disposed on a first edge surface of the memory module, wherein the plurality of contacts are coupled to the buffer device, to communicate with the first integrated circuit ~~device~~ via the buffer device.

14. (original) The memory module of claim 1, wherein the buffer device includes:

transmitter circuit to transmit data onto a signal line coupled to the first contact; and

receiver circuit to receive data from the signal line.

15. (original) The memory module of claim 14, wherein the data transmitted by the transmitter circuit is multiplexed with the data received by the receiver circuit.

16. (original) The memory module of claim 14, wherein the transmitter circuit transmits data and the receiver circuit receives data simultaneously.

17. (original) The memory module of claim 1, wherein the buffer device includes:

unidirectional transmitter circuit to transmit data onto a first signal line disposed on the module; and

unidirectional receiver circuit to receive data from a second signal line disposed on the module.

18. (original) The memory module of claim 1, wherein the buffer device includes:

transmitter circuit to transmit a differential signal that includes encoded clock information;

receiver circuit to receive a differential signal that includes encoded clock information; and

clock and data recovery circuit to extract the clock information encoded with the data received by the receiver circuit.

19. (original) The memory module of claim 1, wherein the connector interface further includes a third contact and a fourth contact, wherein the memory module further includes:

a second integrated circuit having memory including a first storage cell and a second storage cell, wherein:

during the first mode of operation, the first and second storage cells of the second integrated circuit are accessible from the third contact; and

during the second mode of operation, the first storage cell of the second integrated circuit is accessible from the third contact and the second storage cell of the second integrated circuit is accessible from the fourth contact.

20. (original) A memory module comprising:

a connector interface which includes a first contact and a second contact:

a first integrated circuit having memory including a first storage cell;

a second integrated circuit having memory including a second storage cell; and

a buffer device coupled to the first integrated circuit, the second integrated circuit and the connector interface, wherein the buffer device is operable in a first mode and a second mode, wherein:

during the first mode of operation, the first storage cell and the second storage cell are accessible from the first contact; and

during a second mode of operation, the first storage cell is accessible from the first contact and the second storage cell is accessible from the second contact.

21. (original) The memory module of claim 20, wherein the buffer device includes a configurable width interface to communicate with a controller device via the connector interface, wherein the configurable width interface is configured to include a first operable number of interface circuits in the first mode and a second operable number of interface circuits in the second mode.

22. (original) The memory module of claim 21, wherein upon initialization, the buffer device determines an interface configuration of the controller device, wherein the buffer device configures the configurable width interface based on the interface configuration of the controller device.

23. (original) The memory module of claim 21, wherein the memory module includes a programmable storage device, wherein a number of possible configurations of the configurable width interface are specified by information stored in the programmable storage device.

24. (original) The memory module of claim 21, wherein the buffer device includes a control terminal to receive information from the controller device that represents an interface configuration of the controller device, wherein the configurable width is programmed based on the information.

25. (original) The memory module of claim 20, wherein the buffer device includes a programmable register, wherein the first mode and the second mode are specified by respective values stored in the programmable register.

26. (currently amended) The memory module of claim 20, wherein the first and second contacts are included in a plurality of contacts disposed on a first edge surface of the memory module, wherein the plurality of contacts are coupled to the buffer device, to communicate with the first integrated circuit device via the buffer device.

27. (original) The memory module of claim 20, wherein the buffer device includes:
unidirectional transmitter circuit to transmit data onto a first signal line coupled to a controller; and
unidirectional receiver circuit to receive data from a second signal line coupled to the controller.

28. (original) The memory module of claim 20, wherein the buffer device includes:
transmitter circuit to transmit a differential signal that includes encoded clock information;
receiver circuit to receive a differential signal that includes encoded clock information; and
clock and data recovery circuit to extract the clock information encoded with the data received by the receiver circuit.

29. (currently amended) A memory module comprising:

at least one integrated circuit having memory disposed on the memory module; and

a buffer device including:

a memory interface to communicate with the at least one integrated circuit memory device; and

a controller interface to communicate with a controller device, wherein the controller interface includes a configurable number of interface circuits to configure how many parallel signaling paths the controller device uses to access the at least one integrated circuit via the buffer device,

wherein the buffer device includes a serialization circuit coupled to the memory interface and the controller interface, wherein the serialization circuit includes a configurable serialization ratio for data being transferred between the memory interface and the controller interface.

30. (cancelled)

31. (currently amended) The memory module of claim 2930, wherein upon initialization, the buffer device determines the serialization ratio based on an interface configuration of the controller device.

32. (currently amended) The memory module of claim 2930, wherein the memory module includes a programmable storage device, wherein a number of serialization ratios are specified by information stored in the programmable storage device.

33. (currently amended) ~~The memory module of claim 29,~~ A memory module comprising:

at least one integrated circuit having memory disposed on the memory module; and

a buffer device including:

a memory interface to communicate with the at least one integrated circuit memory device; and

a controller interface to communicate with a controller device, wherein the controller interface includes a configurable number of interface circuits to configure how many parallel signaling paths the controller device uses to access the at least one integrated circuit via the buffer device,

wherein the buffer device includes:

unidirectional transmitter circuit to transmit data onto a first signal line coupled to the controller

device; and

unidirectional receiver circuit to receive data from a second signal line coupled to the controller device.

34. (currently amended) ~~The memory module of claim 29,~~ A memory module comprising:

at least one integrated circuit having memory disposed on the memory module; and

a buffer device including:

a memory interface to communicate with the at least one integrated circuit memory device; and

a controller interface to communicate with a controller device, wherein the controller interface includes a configurable number of interface circuits to configure how many parallel signaling paths the controller device uses to access the at least one integrated circuit via the buffer device,

wherein the buffer device includes:

transmitter circuit to transmit a differential signal that includes encoded clock information;

receiver circuit to receive a differential signal that includes encoded clock information; and

clock and data recovery circuit to extract the clock information encoded with the data received by the receiver circuit.

35. (original) An integrated circuit buffer device comprising:

an interface port to communicate with at least one integrated circuit having memory, wherein the interface port includes a first transceiver circuit and a second transceiver circuit;

a configurable port interface to communicate with a controller device, wherein the configurable port interface includes a third transceiver circuit and a fourth transceiver circuit, wherein:

in a first configuration, the first transceiver circuit and the second transceiver circuit are coupled to the third transceiver circuit; and

in a second configuration, the first transceiver circuit is coupled to the third transceiver circuit and the second transceiver circuit is coupled to the fourth transceiver circuit.

36. (original) The integrated circuit buffer device of claim 35, further including a control terminal to receive information from the controller device that represents an interface configuration of the controller device, wherein the configurable port interface is configured based on the information.

37. (original) The integrated circuit buffer device of claim 35, further including a programmable register, wherein the first configuration and the second configuration are specified by respective values stored in the programmable register located on the buffer device.

38. (original) The integrated circuit buffer device of claim 35, further including a control terminal, wherein the first configuration and the second configuration are specified by asserting respective control signals on the control terminal.

39. (original) The integrated circuit buffer device of claim 35, wherein the third transceiver circuit includes:

unidirectional transmitter circuit to transmit data onto a first signal line coupled to the controller device; and

unidirectional receiver circuit to receive data from a second signal line coupled to the controller device.

40. (original) The integrated circuit buffer device of claim 35, wherein the third transceiver circuit device includes:

transmitter circuit to transmit a differential signal that includes encoded clock information;

receiver circuit to receive a differential signal that includes encoded clock information; and

clock and data recovery circuit to extract the clock information encoded with the data received by the receiver circuit.

41.-46. (cancelled)

47. (currently amended) ~~The buffer device of claim 41,~~ A buffer device comprising:

a first interface to communicate with at least one integrated circuit having memory; and

a second interface, coupled to the first interface, to communicate with a controller device, wherein the second interface includes a configurable number of interface circuits to configure how many parallel signaling paths are used to access the at least one integrated circuit via the buffer device,

wherein each interface circuit of the configurable number of interface circuits includes:

unidirectional transmitter circuit to transmit data to the controller device; and

unidirectional receiver circuit to receive data from the controller device.

48. (currently amended) ~~The buffer device of claim 41,~~ A buffer device comprising:

a first interface to communicate with at least one integrated circuit having memory; and

a second interface, coupled to the first interface, to communicate with a controller device, wherein the second interface includes a configurable number of interface circuits to configure how many parallel signaling paths are used to access the at least one integrated circuit via the buffer device,

wherein the second interface includes:

transmitter circuit to transmit a differential signal that includes encoded clock information;

receiver circuit to receive a differential signal that includes encoded clock information; and

clock and data recovery circuit to extract the clock information encoded with the data received by the receiver circuit.

49. (currently amended) A buffer device comprising:

memory interface means for communicating with at least one integrated circuit having memory ; and

controller interface means for configuring how many parallel signaling paths a controller device uses to access the at least one integrated circuit memory via the buffer device,

wherein the controller interface means includes means for transmitting a unidirectional data signal to the controller device and means for receiving a unidirectional data signal from the controller device .

50. (original) The buffer device of claim 49, wherein upon initialization, the buffer device determines an interface configuration of the controller device, wherein the buffer device configures the configurable width interface based on the interface configuration of the controller device.